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Lee D. Whetsel — TI-14124D.3

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Title: IC With Serial Scan Path, Protocol Memory, and Event Circuit

Information Disclosure Statement A

August 27, 2003

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
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Lawrence J. Bassuk, Reg. No. 29,043

Asst. Commissioner for Patents
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Alexandria, VA 22313-1450

Dear Sir:

Applicant requests consideration of all patents, publications or other documents listed on enclosed forms PTO-1449A.

Under Rule 97(h), the filing of this information disclosure statement shall not be construed to be an admission that the information cited in this statement is, or is considered to be material to patentability as defined in Rule 56(b).

Applicant points out particular references and figure numbers and provides a brief explanation of each cited reference in Attachment A.

FEES

Please consider this statement as filed under Rule 97(b) within three months of the filing of a national application, or before the mailing date of a first Office action on the merits, which ever event occurs last. No certification or fee is due. We enclose two copies of this sheet.

Respectfully submitted,

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Attachment A

US Patent Documents

Re. 31,056 to Chau et al. discloses a high speed testing circuit 10 coupled between a test system computer 12 and a device under test 14. The circuit 10 supplies stimuli signals, receives output signals, and provides parametric testing. Same disclosure as US 4,092,589.

US 3,739,193 to Pryor discloses a feedback network where the feedback signal is sufficiently small to be overridden by the input signal.

US 3,789,359 to Clark, Jr., et al. discloses a synchronism indicator for a convolutional decoder.

US 3,824,678 to Harris, et al. discloses a process for laser scribing beam lead semiconductor wafers.

US 3,831,149 to Job discloses a control device having presettable control elements, one for each test lead, each presettable to a desired state for specifying signal-combinations to be monitored. The signal-combinations control the read-in and/or read-out of information from a memory.

US 3,838,264 to Maker discloses a device for checking the contents of a store of a computer that is normally under control of a chain of timing pulses and an address register. The device includes a switching device that sums a quantity of the timing pulses and compares the sum to a known quantity.

US 3,873,818 to Barnard discloses reducing the size of a random access memory storing test patterns. Similar test words are stored as an initial word with indications and binary reconstruction means for generating the other similar test words.

US 3,976,940 to Chau et al. discloses a test circuit 10 including a pair of comparator circuits, each of which is disposed for comparing two minimum threshold amplitudes of responses from a device under test. A multiplexer switches the outputs of the two multiplexers to the device under test.

US 4,023,142 to Woessner discloses a common reliability and service bus connected to each functional unit of LSI apparatus. The bus provides for an addressed unit to go through an operation after a test pattern has been loaded into the unit while the system continues to operate concurrently.

US 4,066,882 to Esposito discloses an automatic computer controlled digital test device that tests circuits by other than random test techniques. The device relies upon software test generation techniques and test programs written in high level test languages and stored on a magnetic disk.

US 4,086,375 to LaChapelle, Jr., et al. discloses a batch process providing beam leads for microelectronic devices having metallized contact pads.

US 4,092,733 to Coontz, et al. discloses an electrically alterable, non-volatile interconnect that selectively connects and disconnects microcircuit elements formed on a wafer. Corresponds to JP 52-136,534.

US 4,108,359 to Proto discloses a device for detecting errors in the execution of a sequence of coded instructions. A feed-back shift register generates a digital sequence combined with the

sequence of instructions to compute a unique sequence check word that is compared to a stored, known good check word.

US 4,146,835 to Chnapko et al. discloses a method of testing the difference in propagation delays through gate circuits of an integrated circuit. The method generates a reference signal at the sensing of the first output of one of the gate circuits and adding a maximum delay time. Any actual signal occurring after the end of the maximum delay time indicates a delay beyond specification.

US 4,161,276 to Sacher, et al. discloses comparing transitions and final logical states of a known good part with a part under test.

US 4,216,539 to Raymond, et al. discloses a programmed processor controlling a set of switches to apply a test signal to a selected node and connect the response from that node to a functional tester.

US 4,242,751 to Henckels, et al. discloses peripherally probing circuit boards and the like with insights into predictable or likely failures and over-riding or discontinuing normal computer back-tracking.

US 4,264,807 to Moen et al. discloses an electric counter including a pair of counter segments connected in cascade. The counters count in Gray code. The second counter segment increments upon the first segment changing from 10 to 00. Corresponds to EP 0017091 and JP 55-135,424.

US 4,268,902 to Berglund, et al. discloses a maintenance interface for interfacing a service processor and a central processor operating synchronously to each other. The interface includes a Level Sensitive Scan Design (LSSD) testing system by degating central processing unit interfaces as required for this testing approach.

US 4,286,173 to Oka, et al. discloses a logical circuit having bypass for testing logical circuits. Corresponds to JP 54-127,245.

US 4,308,616 to Timoc discloses simulating a fault on a selected connection with the output of a shift register in a digital network.

US 4,309,767 to Andow, et al. discloses a monitor system judging the operating condition of an A-D converter from the contents of an adder.

US 4,312,066 to Bantz, et al. discloses an interface between a host processor and a diagnostic/debugging processor the troubleshoot the hardware and software of the host processor. The host uses the LSSD design rules.

US 4,339,710 to Hapke discloses a MOS integrated circuit using field effect transistors including a circuit arrangement for rapidly testing various blocks of the circuit.

US 4,357,703 to Van Brunt discloses performing dynamic testing of complex logic modules at full system clock rates and is resident on each LSI chip under test. The test system includes transmission gates to alter logic paths, and an associated test generator and accumulator at each of the test input and test output.

US 4,365,334 to Smith, et al. discloses producing final test data in response to a stored Logic List for each logic circuit type and stored connection information for a logic circuit under test.

US 4,366,478 to Masuda, et al. discloses a general purpose signal transmitting and receiving apparatus for transmitting and receiving signals between a bilateral bus line and a serial-by-word data transmission line.

US 4,390,969 to Hayes discloses an asynchronous data transmission system with state variable memory and handshaking protocol circuits. The circuit is a stored state circuit including a memory and an output register with an input line and an input request line coupled to the memory and the output register having an output data line and an output acknowledge line.

US 4,426,697 to Petersen, et al. discloses a bus systems with address and status conductors. The address conductor carries mutually spaced serially binary coded bit patterns of m address bits, and the status conductor carries a serial bit pattern or r status bits.

US 4,439,858 to Petersen discloses a digital in-circuit tester for high speed computer control in obtaining high pulse fidelity at each electrical node of a circuit under test. The tester includes a plurality of programmed memory digital test-signal generators responsive to the computer for generating and supplying to the nodes of the circuit under test a complex sequence of digital logic signals. High pulse fidelity is obtained by minimizing the current in the power supply and digital test signal loops.

US 4,483,002 to Groom, Jr., et al. discloses defining a display window for display of signals at selected test points. An operator defines signals at the beginning of the window and at the end of the window, but only after specified conditions. Corresponds to EP 0093229 and JP 58-190784.

US 4,488,259 to Mercy discloses level sensitive scan design strings on an integrated digital logic circuit to provide multiple functions of providing control parameters to logic blocks in the integrated circuit chip, and for providing reconfiguration messages to reconfiguration logic on the integrated circuit chip, in addition to the normal function of transferring test data to various portions

of the integrated circuit chip. This reduces the number of input/output pads on the integrated circuit chip which must be dedicated to these functions.

US 4,493,077 to Agrawal et al. discloses LSI circuits including level sensitive mater latches and slave latches receiving two clock or control signals for normal mode operation. The conditions to initiate the scan testing mode are imposed on the standard clock terminals.

US 4,494,066 to Goel, et al. discloses chips in a module or any second level package. The test mechanism built into each chip will be used in place of mechanical probes to perform a chip-in-place test and interchip wiring test of the package. Level sensitive scan design rules need to be used for each chip and for the package clock distribution network.

US 4,498,172 to Bhavsar discloses a built-in test system that employs a dual-mode feedback shift register to supply test vectors and evaluate test responses of functional and interface networks of a logic system. Test responses are supplied to a quotient bit compressor that generates a system response signature for comparison with an expected fault-free signature to producer a system pass/fail status signal.

US 4,503,536 to Panzer discloses a digital unit testing system using signature analysis. Memory 10 provides test patterns and a memory 12 provides expected test signature patterns. The response data from the unit under test are converted into a signature in signature analyzer 20. Comparator 22 compares the outputs of signature analyzer 20 and memory 12. The test patterns are applied to the unit under test in step with clock 24 and sequential counter 26.

US 4,504,784 to Goel, et al. discloses using Level Sensitive Scan Design rules for testing chips in a packaged structure.

US 4,513,373 to Sheets discloses a local area network using protocol converters 30, 32, 34 and 36 to translate to a computer 52 with an incompatible communications format.

US 4,513,418 to Bardell, Jr. et al. discloses modifying and connecting together in series the LSSD scan paths on a number of logic circuit chips to simultaneously serve as a random signal generator and data compression circuit to perform random stimuli signature generation.

US 4,514,845 to Starr discloses locating a bus fault by placing devices in a high impedance state and sensing current flow between devices.

US 4,519,078 to Komonytsky discloses LSI and discrete logic circuits, including Level Sensitive Scan Design, that incorporate internally generated pseudorandom sequences as test vectors to stimulate the logic circuits under test. Responses to the test vectors are analyzed internally or externally using signature analysis to determine if the circuit has functioned properly.

US 4,553,090 to Hatano et al. discloses a method of testing a logic circuit having a plurality of flip-flops associated with a scan path and combination circuits. The method: transforms parallel input data to serial input data, sets the serial input data in each selected flip-flop, performs a logic operation in the combination circuits on the data stored in the flip-flops, stores the resulting data in the flip-flops and outputs the output data in parallel.

US 4,575,674 to Bass et al. discloses a diagnostic circuit for diagnosing a plurality of serially connected flip-flops in real time. See Figure 2.

US 4,587,609 to Boudreau, et al. discloses a lockout circuit used in an asynchronous shared computer system. A first unit can lock a shareable unit to deny access to other units seeking to lock the shareable unit. Other units can access the shareable unit if they are not seeking to lock it.

US 4,594,711 to Thatte discloses a universal testing block (UTB)for on-chip testing of a VLSI subsystem such as a ROM or an ALU. The UTB can act as a test generator and a test evaluator.

US 4,597,042 to d'Angeac, et al. discloses a device for loading data in, and reading data out of a plurality of latch strings which are contained in a data processing system for testing, failure isolating and initializing. The device is operable to transmit test or initialization data to a plurality of latch strings in a system realized in accordance with the Level Sensitive Scan Design technique.

US 4,597,080 to Thatte, et al. discloses a method and apparatus for testing VLSI processors using a bit-sliced bus-oriented data path including data and control monitors and BIT for the on-chip memory. The control monitor is used to decouple the testing task of the control section from that of the data path.

US 4,598,401 to Whelan discloses a signature analysis circuit. Responses to test patterns applied to the circuit under test are applied to a linear feedback signature register (LFSR). The LFSR produces a signature signal dependent upon its prior state and the responses. The outputs of the LFSR are applied as the address to a memory part having a 1 or 0 output, depending on whether the part tests true or fails. The checking occurs during the testing sequence, in contrast to conventional signature analysis testing where the analysis occurs only at the end of test.

US 4,601,034 to Sridhar discloses an apparatus for testing VLSI memory elements including a parallel signature analyzer.

US 4,602,210 to Fasang et al. discloses a plurality of scan paths in an IC fro testing. Each scan path includes plural bistable scan path flip-flops isolated from the combinational circuits.

US 4,612,499 to Andresen, et al. discloses a test input demultiplexing circuit in which a test signal is multiplexed with a data input line.

US 4,615,029 to Hu, et al. discloses a ring transmission network for interfacing control functions between master and slave devices. A test/maintenance controller 120 interfaces with a slave device 96 through a serial transmission line 106.

US 4,618,956 to Horst discloses testing the inputs of an ALU to see if logical AND is zero or the two inputs are equal whiles allowing the ALU to perform another function at the time the tests are made. Corresponds to EP 0,136,174.

US 4,621,363 to Blum discloses including interface registers in the Level Sensitive Scan Design chain of shift registers. During testing, test data and response data are effected through the interface resisters to the system bus.

US 4,627,018 to Trost, et al. discloses a system to accelerate the granting of prioritized memory requests to a multiport memory system. The system detects one remaining request in the memory, and clears the priority logic before the requestor would normally be activated to receive the next group of memory requests.

US 4,628,511 to Stitzlein, et al. discloses recording pre- and post-failure events to analyze signal activity on an input /output channel to determine failing equipment.

US 4,635,193 to Moyer, et al. discloses a data processor having selective breakpoint capability communicates with a peripheral device to set the breakpoints. The instruction execution control means receive an operand from the peripheral device and selectively store the operand in the instruction register in response to the execution of a breakpoint instruction.

US 4,635,261 to Anderson, et al. discloses plural gates coupled to inputs and outputs of the chip. The gates may asynchronously receive signals from the inputs and asynchronously send signals to the outputs.

US 4,638,313 to Sherwood, et al. discloses addressing for a multipoint communication system for patient monitoring.

US 4,646,298 to Laws, et al. discloses a computer system having intelligent and non-intelligent processing circuits that communicate with one another through connection slots of a communication bus. Each intelligent processing circuit has an identity memory and can specify in the memory that it performed and passed a self-test. The intelligent processing circuits that have passed the self-test arbitrate among themselves, based on their position on the communication bus, to determine which is to become the system test master to test the rest of the system and the non-intelligent processing circuits.

US 4,651,088 to Sawada discloses a logical and electrical characteristics tester having a measuring circuit corresponding to each pin on the device under test.

US 4,669,061 to Bhavsar discloses a scannable flip-flop that can be used in testing combinational logic with test vectors.

US 4,672,307 to Bruer, et al. discloses testing combinatorial circuits by applying 1-transitions to the inputs. The accuracy of the outputs are checked by signature analysis or otherwise. An appropriate Gray code of 1-transistions are obtained from a ring counter and conventional counter.

US 4,674,089 to Poret, et al. discloses an in-circuit emulator (ICE). Capture logic captures the contents of the program address register, the internal data bus and various processor control

lines. Trace circuits use a FIFO buffer to transfer the captures data to the output pins of the chip. A content addressable memory and a software programmable logic array operate as a finite state machine to perform testing.

US 4,679,192 to Vanbrabant discloses an arrangement for an orderly transmission of digital data between stations S1-Sn connected to a common communication path B. A main station distributes clock pulses on the communication path B. The clock pulses are counted in the stations S1-Sn. When the station number and the counting position agree, the relevant station is enabled to transmit data to one of the other stations.

US 4,680,539 to Tsai discloses a linear feedback shift register for inclusion in a level sensitive scan design (LSSD). A scan cell S4 includes a one bit register 23, see Figure 7, two exclusive NOR gates 19 and 20 and additional gates. Corresponds to EP 0148403 and JP 60-147,660.

US 4,680,733 to Duforestel, et al. discloses a device for serializing/deserializing bit configurations of variable length for loading and reading bit configurations in strings of latches.

US 4,687,988 to Eichelberger, et al. discloses applying pseudo-random patterns in parallel to each of the inputs of an IC using LSSD design rules, forming an output signature and comparing the signature to a known good signature.

US 4,694,293 to Sugiyama, et al. discloses a circuit used in an electronic musical instrument in which a number of musical tone generating circuits (receivers) are fed with different tone data by a single control circuit to produce different tones simultaneously.

US 4,698,588 to Hwang, et al. discloses a transparent shift register latch 170 for isolating peripheral ports during scan testing of a logic circuit. See Figure 8. The latch includes internal isolation gate 186.

US 4,701,916 to Naven, et al. discloses an integrated circuit having plural registers. In operation, the registers act as parallel input/output registers. In a shift mode, the registers form a serial shift path and in a test mode, the registers act as a pseudo-random number generator and a signature analyzer.

US 4,701,921 to Powell, et al. discloses a modularized scan path for serially tested logic. Modules 26 each have serial registers 34-40, input gate 48 and output gate 50. Address 16 and control 12 leads connect to address decode/select 52, which selectively connects the scan data in leads 28 and the scan data out leads 30 to the modules for testing. Same disclosure as US 4,710,931 and US 4,710,933.

US 4,710,931 to Bellay et al. discloses a test partionable logic circuit comprising plural functional modules 26a-n. Each functional module interfaces to the exterior of the logic circuit with a data bus 20, an address bus 16 and a control bus 12. Each module is addressable through an address decode/select circuit 52 to operationally isolate the select modules and define a test boundary. Test data is scanned into a serial chain of shift register latches that are connected in a daisy chain configuration. The defines test boundary allows each module to be separately selected and tested to provide a separate and distinct test program for an individual module. Same disclosure as US 4,701,921 and US 4,710,933.

US 4,710,933 to Powell, et al. discloses a parallel to serial scan system for testing logic circuits. Parallel registers 72-80 receive operational and test data from a common bus 70 and are selected by decoder 104. The test data passes through combinational logic and the responses are captured in serial register latches 92-102. Corresponds to US 4,701,921, and US 4,710,931.

US 4,734,921 to Giangano, et al. discloses a fully programmable linear feedback shift register. A polynomial equation is first fed into the linear feedback shift register for setting the respective flip-flops into predetermined logic states, which are used to encode messages to be shifted by the programmable linear feedback shift register. corresponds to WO 88/04097.

US 4,740,970 to Burrows, et al. discloses a specific use of gates in a Built-In Logic Block Observation. Corresponds to EP 0,190,494.

US 4,743,841 to Takeuchi discloses a circuit selectively connecting an operative circuit or a test circuit to the bond pads of an integrated circuit.

US 4,745,355 to Eichelberger, et al. discloses a weighted random pattern testing apparatus and method. The method applies test data to all the inputs in parallel, collects the outputs from all the outputs in parallel, combines the outputs in a signature and compares the signature to a known good, computer simulation generated, signature.

US 4,759,019 to Bently, et al. discloses a programmable fault injection tool for testing a digital processing system. The tool injects faults for a user specified time duration and only after a user specified time delay.

US 4,763,066 to Yeung, et al. discloses comparing four digital test signals to known good reference signals. The four test signals are the result of analog horizontal and vertical signals directed to an integrator/A-D.

US 4,764,926 to Knight et al. discloses an integrated circuit having a built-in self test facility. The combinatorial logic is divided into sub-circuits A-F that are fed and observed by series connected registers flip-flops 1-8. See Figure 3. Multiplexers M4-M6 select the serial input to each

register to include the output of down stream registers. See Figure 7. Corresponds to EP 0195164 and JP 61-155,878.

US 4,777,616 to Moore, et al. discloses a logic analyzer instrument that acquires digital samples from plural logic signals in a main frame computer and displays the edges of the signals enlarged and with precision.

US 4,783,785 to Hanta discloses diagnosis of logical circuits. Input latches 6 capture test data and apply it to combinatorial circuits 5. An output latch 7 captures the response data. Circuit 19 compares the response data to known good data. Corresponds to DE 37 00 251 A1 and JP 62-159,244.

US 4,788,683 to Hester, et al. discloses a converter between a system processor and a support processor for controlling testing of the system processor. A parallel-to-serial and serial-to-parallel converter conveys LSSD test signals between the two processors.

US 4,791,358 to Sauerwald, et al. discloses a method of testing an interconnection between two integrated circuit which are mounted on a carrier and which are interconnected by data connections, for example a printed wiring board. The integrated circuits are also connected to an I^2C serial bus via which test patterns and result patterns can be communicated.

US 4,799,004 to Mori discloses a transfer circuit for operational test of LSI systems. Serial scan registers connected in series shift test data to the inputs of functional blocks 11 and 12 and serial scan registers capture the response data from the functional blocks and shift the response data out.

US 4,799,052 to Near, et al. discloses a method of determining access on an electronic serial bus by implicit token passing. Each device on the serial bus includes a bus access timer that

carries a unique value for that device. Each bus access timer begins counting at an end of transmission signal on the bus and stops either when the count equals a unique count for that device or at a start of transmission signal on the bus.

US 4,800,418 to Natsui discloses an integrated circuit having a reference element selectively operated by an over-voltage applied to a bonding pad.

US 4,801,870 to Eichelberger, et al. discloses using a Level Sensitive Scan Design applying pseudo-random patterns of test signals to a device under test, collecting output responses and comparing the output responses with a know good signature.

US 4,802,163 to Hirabayshi discloses a test facilitating circuit. Serially connected latches F1-F6 are interposed between modules M1-M3.

US 4,808,844 to Ozaki, et al. discloses a bonding pad selection switch circuit connecting a bond pad to an internal circuit in response to a control signal applied to another bond pad.

US 4,811,299 to Miyazawa, et al. discloses a DRAM part that enters a test mode upon the combination of a column address strobe signal, a row address strobe signal and a write enable signal, which normally do not occur together. Corresponds to US 4,992,985, US 5,117,393, and JP 62-250,593.

US 4,812,678 to Abe discloses a through passage circuit selectively short-circuiting an input circuit to an output circuit. Corresponds to DE-A-3,709,032 and JP 62-220879.

US 4,817,093 to Jacobs, et al. discloses testing a multi-chip packaged structure by isolating the one chip under test, applying test signals to that chip, creating a signature of the response signals from that chip and comparing the signature to that of a known good chip.

US 4,819,234 to Huber discloses a debugger, which performs several different functions including identifying and inserting breakpoints, that is part of the operating system of a processor with virtual memory.

US 4,821,269 to Jackson, et al. discloses a diagnostic system for a digital signal processor that monitors various internal test points within several modules. Any test point can be connected to a diagnostic bus for display from an output module.

US 4,825,439 to Sakashita, et al. discloses having an operating mode in which operational signals are output in parallel and a test mode in which serial input test signals can be output in parallel and the operational signals can be output as serial output response signals.

US 4,833,395 to Sasaki, et al. discloses signal generators 11 and 12, input buffer 13 and output buffer 16 for testing a logic circuit 14.

US 4,833,676 to Koo discloses a method and apparatus for testing for stuck open faults in integrated circuits 10 having a plurality of combinational logic devices 18, 20. A chain of shift registers 22 each include latches L1 and L2 for holding respectively the detection test pattern and the initialization test pattern. See the scan cell of Figure 2.

US 4,855,954 to Turner, et al. discloses an in-system programmable device, using non-volatile programmable memory cells, that may be configured or re-configured while installed in a user's device. The normal device inputs and outputs are isolated during programming.

US 4,857,835 to Whetsel discloses a global event qualification system. The system provides the timing and control required to activate an IC's test logic during normal functional operation. The input and outputs of an IC are bordered by unique comparator cells or Event

Qualifier Cells (EQCELL). The EQCELLs compare the data entering or leaving the IC to test data vectors loaded during a scan operation. The EQCELL generates a control signal when the comparison is true. Corresponds to EP 0,315,475.

US 4,860,288 to Teske, et al. discloses a more accurate measurement of clock skew by providing a clock monitor pin directly connected to the clock bus internal to the VLSI chip.

US 4,860,290 to Daniels, et al. discloses a logic circuit having individually testable logic modules. Each of the modules may be selected for testing by means of a scan path in the module made up of serial register latches (SRLs) 34. Each module has a test port 28a.

US 4,862,071 to Sato, et al. discloses high speed circuit testing apparatus having plural test conditions. See Figure 10. Level comparison sections 300 receive an output from circuit under test and reference voltages H and L. The outputs of the level comparison sections 300 become the inputs to logical comparison sections 400. Each logical comparison section 400 includes signal detectors 402 and 403 respectively detecting the presence of the response signal using the strobe pulses STRB 1 and STRB 2.

US 4,862,072 to Harris, et al. discloses a set of four pins of an LSI chip providing access by a serial data line to macrocells or other partitioned logic of the LSI for individual test. The macrocells are connected to the remainder of the logic by a pair of multiplexer/test register combinations, one at the input and one at the output of the macrocell.

US 4,864,579 to Kishida, et al. discloses scan registers provided between circuit blocks.

US 4,866,508 to Eichelberger, et al. discloses, see Figure 4, loading test data into serial latches SR2A and SR2B, passing the test data through the circuits under test, such as latch 21c,

counter 21b and "general" logic 21a, and capturing the resulting test data in serial scan latches SR1A and SR1B.

US 4,870,345 to Tomioka, et al. discloses gate circuits 70-74 connected to the outputs of scan registers 8-13 and 16 to control the input to the next circuit block, such as circuit block 36.

US 4,872,169 to Whetsel discloses a hierarchical scan selection system. A serial scan path can be compressed or expanded to pass only through the desired logic element(s) to be tested. Corresponds to JP 63-085,583.

US 4,875,003 to Burke discloses using a LSSD boundary scan chain to test input and output cells of a circuit.

US 4,878,168 to Johnson, et al. discloses applying serial test information through a serial bus to a storage control unit that interfaces a processor and a storage unit. The control unit changes the serial data from the serial bus to parallel data normally provided by the processor. The test information thus becomes indistinguishable from parallel data applied directly from the processor along a parallel bus.

US 4,879,717 to Sauerwald, et al. discloses testable carriers for integrated circuits. An I^2C serial bus interconnects two integrated circuits and carries test patterns and result patterns with a test device. The serial bus can also be used to test the internal logic circuitry of the integrated circuits.

US 4,887,262 to van Veldhuizen discloses a single-channel bus system for multi-master use with bit cell synchronization, and master station comprising a bit cell synchronization element suitable for this purpose.

US 4,887,267 to Kanuma discloses a logic circuit having a FIFO memory circuit to store values from a test node. The FIFO memory then is unloaded to trace the outputs of such as the states of an internal bus.

US 4,893,072 to Matsumoto discloses an IC tester. The tester applies a test signal to an IC under test and an expected response signal to the input of a shift register. The shift register is clocked to produce the expected response signal at its output at the same time the IC should produce its response to the test signal. The tester then compares the expected response signal to the actual response signal.

US 4,894,830 to Kawai discloses an LSI chip with scanning circuitry for generating reversals along activated logical paths. A pulse is scanned along first flip-flop circuits to propagate test signals through the activated logical paths. A second string of flip-flops connect to the outputs of the logical circuits and are configured into a linear feedback shift register to determine the dynamic performance of the logic circuit.

US 4,896,262 to Wayama, et al. discloses a memory system having a semiconductor memory providing faster access than a magnetic disk storage system.

US 4,899,273 to Omoda, et al. discloses a clock-synchronized simulation method of simulating the logic operations of combination circuits between flip-flops, while operating the flip-flops at a constant time, by using clock signals as conditions for setting and resetting the flip-flops.

US 4,903,266 to Hack discloses a system and method for on-chip self test of memory circuits. The testing includes a random pattern generator addressing all memory locations and using a linear feedback shift register to generate a signature of the test results. A level sensitive scan design serial bus can test all logic and the combination can provide a final test signature.

US 4,910,735 to Yamashita discloses an integrated circuit having plural logic blocks. Each logic block has an operational circuit, a pattern generator, and a switching circuit for selecting either an operational input signal or the pattern signal as the input to the operational circuit. Corresponds to EP 0,273,821.

US 4,912,633 to Schweizer, et al. discloses an hierarchical multiple bus computer system including a master bus and slave buses, which master and slave buses are substantially identical. Communication between the master bus and a slave bus is effected through a combination of an interface controller 12, a shared dual port RAM 14 and a shared RAM controller 13.

US 4,912,709 to Teske, et al. discloses a test system including a ring oscillator distributed around the periphery of the VLSI chip, an I/O cell connected to each signal pin, from which are built the serially connected input registers and output registers.

US 4,918,379 to Jongpier discloses providing an integrated circuit with macro circuits that can be individually tested. A test bus extends along the integrated circuit and connects with a test interface circuit in each macro circuit. The test interface circuits are connected in series.

US 4,926,425 to Hedtke, et al. discloses a system for testing successive component groups separated by accessible nodes. The process observes data at the nodes and supplies test data to the nodes.

US 4,929,889 to Seiler, et al. discloses a test/load bus internal to an integrated circuit to supply test data to test nodes internal of the chip and unload response data from the test nodes.

US 4,930,216 to Nelson discloses a process for preparing integrated circuit dies, while still in wafer form, for surface mounting direct to a substrate without requiring packaging of the dies and maintaining corrosion resistance.

US 4,931,722 to Stoica discloses serial scan paths of registers for serially scanning test data into and out of the registers, applying the serial test data in parallel to combinational logic between the paths and receiving parallel test result data from the combinational logic.

US 4,935,868 to DuLac discloses an integrated circuit for interfacing a standard IEEE 796 bus to a VSB-type buffer bus. the circuit includes a DMA channel for high speed access of the IEEE 796 to the buffer bus and a slave bus channel for high speed access of the buffer bus to the IEEE 796 bus. A third bus interface connects to a local processor to assist in arbitration and control during some types of data transfers.

US 4,937,826 to Gheewala, et al. discloses pre-charging sense lines to known signal levels immediately prior to using the sense lines to sense the signal level at a test point. This eliminates the need for sequential patterns to detect "stuck-open" faults.

US 4,943,966 to Guinta, et al. discloses a serial diagnostic bus (SDB) connecting to a memory control unit. Over the SDB, the system console 30 can read from and write to registers in memory boards 12 and 14.

US 4,945,536 to Hancu discloses connecting input and output signals to a boundary scan register, using three types of boundary scan cells 230, 240 and 250.

US 4,947,106 to Chism discloses a test module testing an analog to digital converter by deterministically checking higher order bits and non-deterministically checking lower order bits.

US 4,956,602 to Parrish discloses wafer scale testing of redundant integrated circuit dies. In Figure 2, wafer test pads 14 are selectively connected by input/output buffer circuit 16 to dies 12 to carry test signals to the dies and carry response signals back to the test pads.

US 4,961,053 to Krug discloses arranging test circuits on a wafer, the wafer also carrying the integrated circuits to be tested. Power is applied to the wafer and testing occurs automatically.

US 4,969,121 to Chan, et al. discloses an integrated circuit programmable logic array circuit with improved microprocessor connectability.

US 4,974,192 to Face, et al. discloses a communications processor 46 for a personal computer. Corresponds to WO-A-8901202.

US 4,974,226 to Fujimori, et al. discloses comparing data stored in a data register 13a with a 1 bit signal stored in a scan latch 1c to determin coincidence or non-coincidence therebetween.

US 4,989,209 to Littlebury et al. discloses an interface apparatus for coupling a multi-channel tester to high pin count integrated circuits. Test stimulus data is applied in parallel to circuits 21 through shift registers 16 and 18. Test response data is assembled in register 17 and returned to tester 11.

US 4,992,985 to Miyazawa, et al. discloses a DRAM starting and stopping testing by a combination of a column address strobe, row address strobe and write enable signal.

US 5,001,713 to Whetsel discloses an event qualification testing architecture. A boundary test architecture uses input and output test registers 12,22 having functions controlled by an event qualifying module (EQM) 30. In response to the EQM receiving a matching condition signal from the register 22, the EQM may control the test registers 12,22 to perform a variety of tests on the incoming and outgoing data. The internal functional logic 20 may continue to operate at speed during the testing to determine faults not otherwise discoverable. Corresponds to US 5,103,450, EP 0,382,360, and JP 30-20683.

US 5,008,885 to Huang, et al. discloses inserting errors into parts at controlled times through programmable masks.

US 5,014,186 to Chisholm discloses a data processing system having a bus system coupling I/O units to a storage unit. The I/O units are supplied a line size signal representing the line size of the storage unit. The I/O units respond to this line size signal to adjust the data transfer size or packet of the I/O unit to match the storage unit line size.

US 5,023,872 to Annamalai discloses simple error detection logic with an error counter and a timer detects errors in a dual token ring network.

US 5,042,005 to Miller, et al. discloses a timer circuit with match recognition features.

US 5,051,996 to Bergeson, et al. discloses a built-in test by signature system that provides fault detection by the bits in the signature detection logic.

US 5,053,949 to Allison, et al. discloses a debug peripheral that uses externally provided instructions to control a core processing unit.

US 5,056,094 to Whetsel discloses a delay fault testing system. A special test instruction to a boundary test cell invokes a toggle mode that allows the output boundary of an IC to output a transition between logic states on the edges of a clock signal. The same test instruction configures a boundary test cell of a receiving IC to sample input data on the subsequent edge of the clock signal. The sampled data can be inspected to determine whether the output signal propagated to the receiving IC in the prescribed time.

US 5,084,814 to Vaglica, et al. discloses a CPU having access to on-chip and off-chip peripherals and memory in both a normal and alternate mode of operation by means of a parallel bus, which it operates as a bus master. In an alternate mode, the CPU receives instructions on a serial bus on which the CPU is a slave device.

US 5,084,874 to Whetsel discloses a testing buffer register 12. See Figure 2. The test cell can also include compare and other logic. See Figures 6 and following. Corresponds to US 5,495,487; US 5,602,855; US 5,631,911; US 6,081,916; and US 6,304,987.

US 5,128,664 to Bishop discloses a search technique for identifying slave devices connected to a serial bus. When a master controller senses a condition that requires a condition that requires an assessment of devices on the bus, it examines the addresses of previously connected devices at more frequent time intervals than it does for addresses that were not previously associated with connected devices.

US 5,133,062 to Joshi, et al. discloses a RAM buffer controller for providing simulated first-in first-out (FIFO) buffers in a random access memory.

US 5,155,432 to Mahoney discloses a system for scan testing of logic circuit networks. Switching means are selectively varied to provide different test circuit configurations for different modes of operation.

US 5,159,465 to Maemura, et al. discloses a facsimile machine having a transmission speed selective downshift function. A common buffer memory provides for temporarily storing coded image information either in an Error Correction Mode or a normal transmission mode.

US 5,167,020 to Kahn, et al. discloses a serial data transmitter with dual buffers operating separately and having scan and self test modes.

US 5,187,795 to Balmforth, et al. discloses a pipelined signal processor having plural bi-directional configurable parallel ports that are configurable as individual ports or as coupled pairs of ports.

US 5,214,760 to Hammond, et al. discloses an adaptable multi-port data buffer.

US 5,218,702 to Kirtland discloses a system for selecting request for a resource before decoding of requested resource address and validating selection thereof.

US 5,276,807 to Kodama, et al. discloses bus interface synchronization circuitry for reducing time between successive data transmission in a system using an asynchronous handshake.

US 5,303,148 to Mattson discloses a voice recognition system for doctors in surgery. The machine compares received audio to stored known words and displays the words on a screen.

US 5,329,471 to Swoboda et al. discloses an emulation system using state machines for a microprocessor. The system provides emulation, simulation and testability without physical probing or special test fixtures. The system provides a serial scan testability interface having first and second scan paths. The first scan path is provided for applying digital information to the functional circuit for use in emulation of the functional circuit. The second scan path connects to state machine circuits that have a sequence of states responsive to the emulation command codes. The disclosed system also incorporates a JTAG interface and has different clock signal domains.

US 5,495,487 to Whetsel corresponds to US 5,084,874.

US 5,602,855 to Whetsel corresponds to US 5, 084,874.

US 5,905,738 to Whetsel discloses a digital bus monitor (DBM) circuits 20,22. The DBM circuits observe data on address bus 14, data bus 16 and control bus 18 while the buses are in a functioning mode. The DBM circuits include memory and compare circuits. In response to a matching condition, an event qualification module may perform a variety of tests on incoming data while the buses continue to operate at speed. Corresponds to US 6,131,171.

Foreign Patent Documents

EP 0,136,174 A3 (European patent application) to Horst discloses circuits 22 performing the functional equivalent of ALU tests, such as mask and zero detect, while the ALU is performing its function.

EP 0,148,403 A3 (European patent application) to Tsai discloses a linear feedback shift register that can be programmed into an LSSD test mode, to generate test patterns for a VLSI circuit, or to perform a corresponding signature analysis on hashing functions on a VLSI response to the test pattern.

EP 0,190,494 A1 (European patent application) to Burrows, et al. discloses a known Built-In Block Observation or BILBO circuit, Figure 1, modified, as depicted in Figure 3, selectively to feed the data output into the data input.

EP 0,195,164 A1 (European patent application) to Knight, et al. discloses an integrated circuit having built-in test facility. The IC is partitioned into a number of sub-circuits, each of which comprises a combinatorial logic circuit and a register. Each combinatorial circuit has its inputs coupled to at least one register and has its outputs coupled to at least one register. The output of the IC is taken from one or more registers. The registers are selected to initiate a test operation for the testing of the IC.

EP 0,273,821 A2 (European patent application) to Yamashita discloses testing a wafer 30 of integrated circuits 31-39. Each IC includes an operating circuit 42, a pattern generating circuit 40, a switching circuit 41 for selecting a data input or the pattern generating circuit as the input to the operating circuit 42 and a data compressing circuit 43.

EP 0,310,152 A2 (European patent application) to Wood discloses a synchronous test overlay circuit, Figure 3, interposed between blocks of logic to be tested.

JP 01-038674 A discloses eliminating the need for an additional input terminal for testing by providing a test recognition circuit 9.

JP 01-043773 (A) to Koji discloses testing a propagation delay to a flip-flop 104 by selecting the output of flip-flop 104 with a scan-address pin 112 to obtain the state of the flip-flop 104 output on scan-out pin 116.

JP 01-068167 A discloses a fault detection processor. Signal checking means 2 detects the presence and absence of an error. Fault occurrence calculation means 3 calculates a fault occurrence frequency PF. Device test start means 4 starts a devices test circuit 9 as the frequency PF is a prescribed value or more.

JP 57-094857 A apparently discloses a scan path 471-472 with three sets of latches 400-403, 410-413, and 430-433. Addresses are supplied to latches 400-403. The contents of the scratch pad memory is read to latches 430-433, which are then observed by shifting.

JP 57-209546 (A) discloses flip-flops 2-1 through 2-n, storage registers 3A and 3B, multiplexers 4A, 4B and 4C, a comparison condition setting flip-flop 5 and a comparison circuit 6. Storage registers 3A and 3B contain scanning addresses loaded externally. Multiplexers 4A and 4B

selectively output the contents of the flip-flops 2-1 through 2-n according to the addresses stored in them. Multiplexer 4C outputs the contents of the selected flip-flop according to the addresses present on address line l.

JP 58-155599 to Wada, et al. discloses a memory testing circuit.

JP 58-191021 A discloses detecting a fault in comparator 3 by comparing the received input interface 2 with a standard input stored in memory 1.

JP 59-210382 (A) discloses testing an LSI circuit with scan-in flip-flops 23aa-23ag and scan-out flip-flops 23ba-23br. Testing device 1 provides an address decoded in decoder 25 to select one scan-in and one scan-out flip-flop. The outputs of the flip-flops are connected through an OR gate 26 to a testing device, which compares the outputs to decide whether the LSI is normal.

JP 60-140834 discloses that the comparison circuit 2 compares the outputs of the 4 bit register 1 with the expected data outputs of register 3.

JP 60-0252958 discloses scan flip-flops 35a-35c in each input/output circuit unit 31. Necessary data are transmitted in series using a small number of connecting lines distributed by a decoder 34.

JP 60-262073 discloses monitoring the operation of digital signal processor 1 by simulation processor. Input data on input signal line IL is stored in memory 6. Output from the digital signal processor 1 is stored in memory 7. Simulation processor 8 processes the data from memory 6 and the output of processor 8 is compared in comparator 3 with the data stored in memory 7. Non-coincidence causes a signal on terminal 5.

JP 62-031447 A discloses monitoring and recording data on a data bus independent of a computer to be monitored. The monitored data is compared with other data to determine stop conditions.

JP 62-228177 (A) discloses circuits 11-13 that capture the logical states on terminals 1-4. The contents of circuits 11-13 can be clocked out on terminal 23 by placing a low on terminal 4.

JP 62-280663 discloses logic circuit 110. Fault detection circuits 121-12n detect faults in logic circuit 110 at particular locations. Flip-flops 141-14n save the detected fault state through selectors 131-13n. Logic circuit 150 receives the outputs of flip-flops 141-14n and produces a fault signal at terminal C.

JP 63-073169 (A) discloses reducing by one pin the number of pins used for normal and test operation. Pin 6 is multiplexer for both data and test.

JP 63-188783 A discloses a logic analyzer. A detector 10 detects a prescribed logic relation among plural binary inputs. Time width detection part 20 determines whether the prescribed logic relation occurs for a prescribed time. Selection part 30 selects a prescribed input signal to be analyzed.

JP 63-213014 A discloses shift path control means 100 passing an instruction to clock transmission instruction means 200 that controls transmission of a clock signal to each of 1st shift path logical units 400,410, 2nd shift path logical units 420,430,440, and 3rd shift path logical unit 450.

JP 63-310046 A discloses a test auxiliary circuit. The circuit reduces a serial shift operation to read out response data of a circuit to be tested by latching data at an input terminal to a latch circuit only when the data at a parallel input terminal differs from expected value data.

JP 64-006572 discloses in Figure 1 an Exclusive-OR gate 8 receiving the outputs of input shift registers 2 and output shift registers 5.

JP 64-079673 to Masao discloses testing a RAM circuit.

WO 88/04097 to Giangano, et al. discloses a fully programmable linear feedback shift register having plural blocks of flip-flop shift registers. A polynomial equation is fed into the entire circuit to set the flip-flops to desired logic states to code a message passed through the linear feedback shift register.

Other Documents

The Avra paper discloses a test and maintenance control block that receives commands serially over an ETM-BUS to control chip level test and maintenance features such as chip initialization, serial scan, debug and built-in self-test operations.

The Bhavsar, et al. paper (1981) discloses self testing by polynomial division in feed back shift registers for test vector generation and response evaluation.

The Breuer, et al. paper discloses a module test and maintenance controller (MMC) for testing chips. The controller tests every chip in a module by an ETM-BUS or a Boundary Scan bus. The MMC requires either a RISC-type processor or DMA controller.

The Dervisoglu paper discloses an architecture for implementing scan technology for test and debug in a sate-of-the-art workstation.

The El-ziq, et al. paper discloses a mixed-mode built-in self-test technique using scan path and signature analysis.

The ETM-Bus Specification paper discloses the performance requirements for a particular test bus.

The Haedtke, et al. paper discloses multilevel self-test for the factory and field. Figure 4 depicts a simplified bi-directional boundary scan I/O cell.

The Hahn, et al. paper discloses VLSI testing by on-chip error detection with scanned and expected data being latched in respective latches. The outputs of the two latches connect to an exclusive OR gate to determine any error.

The Hudson, et al. paper, September, 1987, discloses parallel self test with pseudo-random test patterns.

The Hudson paper discloses integrating BIST and boundary scan on a board.

The IBM Technical Disclosure Bulletin, June, 1985, discloses a bi-directional double latch that can be used in Level Sensitive Scan Designs.

The IBM Technical Disclosure Bulletin, December, 1988, discloses a self-contained performance monitor for a personal computer. The monitor interrogates the PC I/O for 2 programmable events and 1 external event. When an event occurs, a timer value, the PC data bus, and identification information are captured and automatically gated into a battery-back-up RAM. The RAM is read through a register 60 connected to a register bus.

The Joint Test Action Group paper, January, 1988, discloses an early version of the standard for a boundary scan test architecture.

The Laurent paper discloses implementing a boundary scan path and an internal scan path in VLSI circuits. Figures 2 and 3 depict respective input and output buffers.

The Lien paper discloses a Module test and Maintenance Controller (MMC) that can test every chip on a JTAG boundary scan bus and control more than one test bus. The MMC includes a test-channel that, once initialized by the MMC processor, controls testing across a specific test bus.

The Marlett, et al. paper discloses a RISP methodology for testing integrated circuits.

The Maunder et al. paper discloses an industry-standard boundary-scan framework for merchant and custom integrated circuits. The boundary-scan path provides for external, internal and self-testing of integrated circuits through shift register-latch scan-cells located at the bond pads of the integrated circuit. Figure 9 depicts one possible implementation of a scan-cell complying with JTAG requirements. The paper also discloses testing analog signals.

The Ohletz, et al. paper discloses investigating the overhead for different scan designs and self-testing designs.

The Ohsawa, et al. paper discloses a 4 Mbit CMOS DRAM with built-in self-test. A board carrying 64 4 Mbit x 1 DRAMs provides for simultaneous testing of all DRAMs in one row.

The Paraskeva, et al. paper discloses a new structured test register for VLSI self-test. See Figure 1.

The Pradhan et al paper discloses a circular BIST technique to perform a random test of sequential logic. Additional deterministic tests are presented to the circuit under test by configuring the circular path as a partial scan chain.

The Russell paper discloses the JTAG proposal and it impact on automatic testing. Figure 2 depicts an input pin cell and Figure 3 depicts an output pin cell.

The Sabo paper discloses the costs of not designing for test.

The Sellers, et al. book extract illustrates four ways to design an error correction circuit in Figures 12.2a-12.2d.

The van Riessen, et al. paper discloses integration of the boundary scan standard with the built-in self test approach. The built-in self test uses a macroprocessor, see Figure 7 to produce a test signature.

The Wagner paper discloses interconnect testing with boundary scan. Figure 4 depicts a boundary scan bit-slice.

The Wang, et al. 1986 paper discloses a concurrent built-in logic block observer combines the scan and BILBO techniques.

The Wang, et al. 1989 paper discloses using a JTAG boundary scan bus with pseudorandom patterns from a cellular automaton to locate defective chips and walking sequences to locate bad interconnects.

The Whetsel paper, January, 1988, discusses the details of the JTAG port and architecture. Figure 8 depicts a boundary register bit.

The Whetsel paper, July, 1988, discloses a standard test bus and boundary scan architecture used by Texas Instruments Incorporated in its implementation of the JTAG architecture. The disclosure covers the scan path, a scan cell, a test access port and instruction and data registers, and state diagrams.

The Whetsel paper, October, 1988, discloses a proposed standard test bus and boundary scan architecture from the Joint Test Action Group.

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TI-14124D.3	div. of 09/597,472

APPLICANT: Lee D. Whetsel

FILING DATE	GROUP
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U.S. PATENT DOCUMENTS

+EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
		Re. 31,056	10/12/1982	Chau, et al.	324	73 R	5/28/1980
		3,739,193	6/12/1973	Pryor	307	205	1/11/1971
		3,789,359	1/29/1974	Clark, Jr., et al.	340	146.1D	10/4/1972
		3,824,678	7/23/1974	Harris, et al.	29	578	8/31/1970
		3,831,149	8/20/1974	Job	340	172.5	2/14/1973
		3,838,264	9/24/1974	Maker	235	153 AM	11/23/1971
		3,873,818	3/25/1975	Barnard	253	153 AC	10/29/1973
		3,976,940	8/24/1976	Chau, et al.	324	73 R	2/25/1975
		4,023,142	5/10/1977	Woessner	340	172.5	4/14/1975
		4,066,882	1/3/1978	Esposito	235	302	8/16/1976
		4,086,375	4/25/1978	LaChapelle, Jr., et al.	427	90	11/7/1975
		4,092,733	5/30/1978	Coontz, et al.	365	200	5/7/1976
		4,108,359	8/22/1978	Proto	235	304	3/30/1977
		4,146,835	3/27/1979	Chnapko, et al.	324	73 R	3/8/1978
		4,161,276	7/17/1979	Sacher, t al.	235	302	3/1/1978
		4,216,539	8/5/1980	Raymond, et al.	371	20	5/5/1978
		4,242,751	12/30/1980	Henckels, et al.	371	26	2/24/1976
		4,264,807	4/28/1981	Moen, et al.	235	92 GD	4/9/1979
		4,268,902	5/19/1981	Berglund, et al.	364	200	10/23/1978
		4,286,173	8/25/1981	Oka, et al.	307	440	3/27/1978
		4,308,616	12/29/1981	Timoc	371	23	5/29/1979
		4,309,767	1/5/1982	Andow, et al.	371	24	8/21/1979
		4,312,066	1/19/1982	Bantz, et al.	371	16	12/28/1979
		4,339,710	7/13/1982	Hapke	324	73 R	2/12/1979
		4,357,703	11/2/1982	Van Brunt	371	15	10/9/1980
		4,365,334	12/21/1982	Smith, et al.	371	27	2/9/1981
		4,366,478	12/28/1982	Masuda, et al.	340	825	1/5/1981
		4,390,969	6/1/1983	Hayes	395	550	4/21/1980
		4,426,697	1/1/1984	Petersen, et al.	340	825.52	1/24/1981
		4,439,858	3/1/1984	Petersen	371	20	5/28/1981
		4,483,002	11/13/1984	Groom, Jr., et al.	371	29	4/19/1982
		4,488,259	12/11/1984	Mercy	364	900	10/29/1982
		4,493,077	1/8/1985	Agrawal, et al.	371	25	9/9/1982
		4,494,066	1/15/1985	Goel, et al.	324	73 R	7/2/1981

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		4,498,172	2/5/1985	Bhavsar	371	25	7/26/1982
		4,503,536	3/5/1985	Panzer	371	25	9/16/1982
		4,504,784	3/12/1985	Goel, et al.	324	73R	7/2/1981
		4,513,373	4/1/1985	Sheets	364	200	12/28/1982
		4,513,418	4/23/1985	Bardell, Jr, et al.	371	25	11/8/1982
		4,514,845	4/30/1985	Starr	371	15	8/23/1982
		4,519,078	5/21/1985	Komonytshy	371	25	9/29/1982
		4,553,090	11/12/1985	Hatano, et al.	324	73 AT	7/23/1980
		4,575,674	3/11/1986	Bass, et al.	324	73 R	7/1/1983
		4,587,609	5/1/1986	Boudreau, et al.	395	726	7/1/1983
		4,594,711	6/10/1986	Thatte	371	25	11/10/1983
		4,597,042	6/24/1986	d'Angeac	364	200	9/13/1983
		4,597,080	6/24/1986	Thatte, et al.	371	25	11/14/1983
		4,598,401	7/1/1986	Whelan	371	25	6/25/1984
		4,601,034	7/15/1986	Sridhar	371	25	3/30/1984
		4,602,210	7/22/1986	Fasang, et al.	324	73	12/28/1984
		4,612,499	9/16/1986	Andresen, et al.	324	73 R	11/7/1983
		4,615,029	9/30/1986	Hu, et al.	370	89	12/3/1984
		4,618,956	10/21/1986	Horst	371	68	9/29/1983
		4,621,363	11/4/1986	Blum	371	25	12/6/1984
		4,627,018	12/1/1986	Trost, et al.	395	476	9/8/1983
		4,628,511	12/9/1986	Stitzlein, et al.	371	22	2/25/1982
		4,635,193	1/6/1987	Moyer, et al.	364	200	6/27/1984
		4,635,261	1/6/1987	Anderson, et al.	371	25	1/26/1985
		4,638,313	1/20/1987	Sherwood, et al.	340	825.52	11/8/1984
		4,646,298	2/1/1987	Laws, et al.	371	16	5/1/1984
		4,651,088	3/17/1987	Sawada	324	73R	5/6/1985
		4,669,061	5/26/1987	Bhavsar	365	154	12/21/1984
		4,672,307	6/9/1987	Breuer, et al.	324	73 R	12/20/1985
		4,674,089	6/16/1987	Poret, et al.	371	25	4/16/1985
		4,679,192	7/1/1987	Vanbrabant	340	825.52	1/24/1986
		4,680,539	7/14/1987	Tsai	324	73	12/30/1983
		4,680,733	7/14/1987	Duforestel	364	900	10/29/1984
		4,687,988	8/18/1987	Eichelberger, et al.	324	73 AT	6/24/1985
		4,694,293	9/15/1987	Sugiyama, et al.	340	825.68	9/16/1985

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		4,701,916	10/20/1987	Naven, et al.	371	15	3/17/1986
		4,701,921	10/20/1987	Powell, et al.	371	25	10/23/1985
		4,710,931	12/1/1987	Bellay, et al.	371	25	10/23/1985
		4,710,933	12/1/1987	Powell, et al.	371	25	10/23/1985
		4,734,921	3/29/1988	Giangano, et al.	377	72	11/25/1986
		4,740,970	4/26/1988	Burrows, et al.	371	15	12/11/1985
		4,743,841	5/10/1988	Takeuchi	324	73 R	5/20/1985
		4,745,355	5/17/1988	Eichelberger, et al.	324	73 R	5/11/1987
		4,759,019	7/19/1988	Bentley, et al.	371	3	7/10/1986
		4,763,066	8/9/1988	Yeung, et al.	324	73R	7/23/1986
		4,764,926	8/16/1988	Knight, et al.	371	25	12/11/1985
		4,777,616	10/11/1988	Moore, et al.	364	900	5/12/1986
		4,783,785	11/8/1988	Hanta	371	25	1/5/1987
		4,788,683	11/29/1988	Hester, et al.	371	20	1/14/1986
		4,791,358	12/13/1988	Sauerwald, et al.	324	73 R	9/2/1986
		4,799,004	1/17/1989	Mori	324	73 R	1/25/1988
		4,799,052	1/1/1989	Near, et al.	340	825.52	1/13/1986
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APPLICANT: Lee D. Whetsel

FILING DATE	GROUP
August 27, 2003	TBD

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		4,870,345	9/26/1989	Tomioka, et al.	371	22.3	8/3/1987
		4,872,169	10/3/1989	Whetsel, Jr.	371	22.3	3/6/1987
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		4,899,273	2/6/1990	Omoda, et al.	364	200	12/10/1986
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		4,947,106	8/7/1990	Chism	324	73.1	3/31/1988
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		5,001,713	3/19/1991	Whetsel	371	22.3	2/8/1989
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		APPLICANT: Lee D. Whetsel	
		FILING DATE: August 27, 2003	GROUP: TBD

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In the United States Patent and Trademark Office

In re the Application of
Lee D. Whetsel — TI-14124D.3

Div of Serial No: 09/597,472 — Art Unit: TBD

Filed: August 27, 2003 — Examiner: L. Hua

Title: IC With Serial Scan Path, Protocol Memory, and Event Circuit

Information Disclosure Statement B

August 27, 2003

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as Express Mail #EV333321448US in an envelope addressed to: Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on August 27, 2003.

Lawrence J. Bassuk, Reg. No. 29,043

Asst. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant requests consideration of all patents, publications or other documents listed on enclosed forms PTO-1449B.

The references listed on the forms PTO-1449B result from two sources. An Arlington, Virginia searcher located several of these references in a search of subject matter similar to that presently claimed. The remaining references arose from licensing negotiations on claims in US 5,103,450, particularly claim 1.

Under Rule 97(h), the filing of this information disclosure statement shall not be construed to be an admission that the information cited in this statement is, or is considered to be material to patentability as defined in Rule 56(b).

Applicant points out particular references and figure numbers and provides a brief explanation of each cited reference in Attachment A.

FEES

Please consider this statement as filed under Rule 97(b) within three months of the filing of a national application, or before the mailing date of a first Office action on the merits, which ever event occurs last. No certification or fee is due. We enclose two copies of this sheet.

Respectfully submitted,

Lawrence J. Bassuk
Reg. No. 29,043
Attorney for Applicant

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, Texas 75265
972-917-5458

In the United States Patent and Trademark Office

In re the Application of
Lee D. Whetsel TI-14124D.3

Div of Serial No: 09/597,472 Art Unit: TBD

Filed: August 27, 2003 Examiner: L. Hua

Title: IC With Serial Scan Path, Protocol Memory, and Event Circuit

Information Disclosure Statement B

August 27, 2003

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as Express Mail #EV333321448US in an envelope addressed to: Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on August 27, 2003.

Lawrence J. Bassuk, Reg. No. 29,043

Asst. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Respectfully submitted,

Lawrence J. Bassuk
Reg. No. 29,043
Attorney for Applicant

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Attachment A

US 4,577,318 to Whitacre, et al., discloses comparing A data on the 26 lines of data set A with B data on the 26 lines of data set B. The lines of A data and the lines of B data are fed to selector multiplexers 505a and 505b. The outputs of these multiplexers are fed to an EOR circuit 502 for comparison.

A mask register 501 connects to the selector multiplexers in order to blank out selected input lines to multiplexers 505a,b. Mask register 501 has an input CI bus 501ci, which carries the bus control signals from bus control unit 510, which in turn connects to the D or data bus 34.

The present claims distinguish over the cited art by requiring a protocol selection memory to be coupled to a serial scan path or a serial data input lead and requiring an event circuit to be coupled to the protocol selection memory.

US 4,635,261 to Anderson, et al., discloses an on chip test system for configurable gate arrays. In Figure 3, input shift registers 23 and output shift registers 25 are connected in series to provide test signals to the outputs of the circuit 20, to connect to further circuits through bond pad 36 and to provide self test of the shift registers themselves.

In Figure 4, input registers 23 are connected together to form a pseudo-random pattern generator 30 with outputs connected to the gates 21. The output registers 25 are connected in series to form a signature analysis register 40 receiving the outputs from the gates 21.

The present claims distinguish over the cited art by requiring a protocol selection memory to be coupled to a serial scan path or a serial data input lead and requiring an event circuit to be coupled to the protocol selection memory.

US 4,857,835 to Whetsel appears not to be prior art to this application. This patent is to the same inventor as in this application. It issued on August 15, 1989. The present application claims priority to an application filed on June 30, 1989.

US 4,893,072 to Matsumoto, et al., discloses testing an IC device 21 that includes a logic circuit section L and a memory circuit section M. Logic circuit section L includes flip-flops 30, 31, 32, and 33 that provide time delays between input and output signals through the IC 21. An IC-device testing apparatus 23 includes flip-flop circuits F11, F21, F22, ..., Fnn, that provide for matching the time delays through the logic circuit section L of actual test signals applied to the IC 21 and expected signals EX.

The present claims distinguish over the cited art by requiring a protocol selection memory to be coupled to a serial scan path or a serial data input lead and requiring an event circuit to be coupled to the protocol selection memory.

US 5,001,173 to Whetsel appears not to be prior art to this application. This patent is to the same inventor as in this application. It issued on March 19, 1991. The present application claims priority to an application filed on June 30, 1989.

US 5,170,398 to Fujieda, et al., appears not to be prior art to this application. This patent results from an application filed July 18, 1990. The present application claims priority to an application filed on June 30, 1989.

US 5,353,308 to Whetsel appears not to be prior art to this application. This patent is to the same inventor as in this application. It issued on October 4, 1994.

US 5,623,500 to Whetsel appears not to be prior art to this application. This patent is to the same inventor as in this application. It issued on April 22, 1997.

US 6,457,148 to Yoshiba appears not to be prior art to this application. It results from an application filed on February 9, 1999.

US 6,601,193 to Liebau appears not to be prior art to this application. It results from an application filed on August 3, 2000.

US 2003/0140295 to Antley, et al., appears not to be prior art to this application. It results from an application filed on January 16, 2003.

US 2002/0194565 to Arabi appears not to be prior art to this application. It results from an application filed on June 18, 2001.

Foreign patents

European patent application EP 0,315,475 appears not to be prior art to this application. This publication is to the same inventor as in this application and corresponds to US 4,857,835, mentioned above. It was published on May 10, 1989.

Other references

The Intel Microprocessor and Peripheral Handbook, 1988, Section 2.11.2 TLB Testing, discloses that there are two TLB testing operations. One is to write entries into the TLB. The other is to perform TLB lookups. C: is the command bit. A "0" written into this bit causes an immediate write into the TLB entry. A "1" written into this bit causes an immediate TLB lookup.

The present claims distinguish over the cited art by requiring a protocol selection memory to be coupled to a serial scan path or a serial data input lead and requiring an event circuit to be coupled to the protocol selection memory.

The Intel 80386 Programmer's Reference Manual, 1986, in Figure 12-1, discloses 4 breakpoint linear address registers.

The Kuban, et al. article discloses, page 39, column 3, first full paragraph, that the operating mode of the MC6804P2 is controlled by RESET, MDS, PA7, and PA6. When RESET is brought high, the levels on the MDS, PA7, and PA6 pins are sampled, and the appropriate mode is selected. The two self-test modes are invoked by a high on the MDS and PA7 pins.

The functional test is entered if the PA6 pin is low; otherwise, a high on PA6 invokes the ROM verify test.

The present claims distinguish over the cited art by requiring a protocol selection memory to be coupled to a serial scan path or a serial data input lead and requiring an event circuit to be coupled to the protocol selection memory.

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U.S. PATENT DOCUMENTS

+EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
		4,635,261	1/6/1987	Anderson, et al.	371	25	1/26/1985
		4,857,835	8/15/1989	Whetsel, Jr.	324	73	11/5/1987
		4,893,072	1/9/1990	Matsumoto	371	223	6/22/1988
		5,001,713	3/19/1991	Whetsel	371	22.3	2/8/1989
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		5,353,308	10/4/1994	Whetsel, Jr.	371	22.3	8/6/1990
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		US 2002/0194565 A1	12/19/2002	Arabi	714	729	6/18/2001
		US 2003/0140295 A1	7/24/2003	Antley, et al.	714	733	1/18/2002

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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
		EP 0,315,475 A2	1/1/1986	Europe	G01	R31/28	X

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OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		Kuban, John R. and Bruce, William C, "Self-Testing the Motorola MC6804P2," pp. 33-41, 1984 IEEE, October 1983	
		Intel, 80386 "Programmer's Reference Manual, Chapter 12: Debugging," pp 12-1 - 12-9, 1986	
		Intel, Intel Microprocessor and Peripheral Handbook, 1988, "Chapter 2.11 Testability"	

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